Solving Structured Electronic Design of Negative Feedback Amplifiers as Nonlinear Programming Problems

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Abstract

This paper searches the best solution for the stages of noise and bandwidth of negative feedback amplifiers by resorting to Structured Electronic Design, through optimization methods. On one side, noise optimization is achieved by establishing the noise-characteristic as a function of bias current. On the other side, bandwidth optimization is obtained by establishing the equation for the open loop gain pole-product (LP product). Both aspects are defined as nonlinear programming (NLP) problems, where the design variables are related with the parameters of the device (bipolar transistors) used to synthesize the amplifiers. Differential Evolution is used to solve the noise NLP problem and the Hooke-Jeeves method is used to solve the bandwidth NLP problem. The obtained results are presented and some conclusions are established.

1 Introduction

Nowadays, some activities in engineering design are still lead by experience. Regarding Electronics, Structured Electronic Design is a methodology that starts from a set of assumptions and rules. A step-by-step modification of an ideal solution is performed until a real solution, which satisfies all initial requirements, is generated. In the present work, we will focus in the case of negative feedback amplifiers.

The negative feedback amplifiers are composed of an active circuit connected to a feedback network built by passive devices (see Figure 1). The active circuit is implemented by a nullor, which is synthesized by transistors, while the spec's are kept [8]. The main aspects of design to be considered are: noise, distortion and bandwidth. The way a solution (design) is found rests on a search based on an ideal solution (the nullor), and by applying a synthesis procedure, the ideal solution is converted into a real one that fulfills the specifications [9]. Noise, distortion and bandwidth are the user specifications; subsequently these have to be satisfied when the new amplifier is designed.

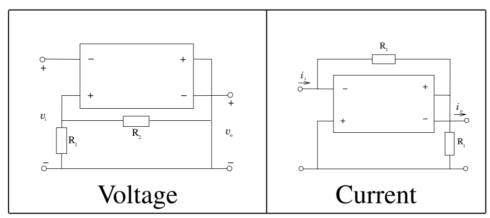

Figure 1. Voltage and current amplifier with resistive devices on the feedback network.

In this work, two of the three design stages: (1) noise and (2) bandwidth are modeled as NLP problems and solved with two techniques. The aim is to avoid designer-participation in the process and to let the optimization techniques do the search for the best design values (this activity is typically made by the designer) in Structured Electronic Design. To the best of our knowledge, this is the first attempt to solve Structured Electronic Design stages as NLP problems.

This paper is organized as follows: Section 2 presents an introduction to Structured Electronic Design, Section 3 includes the steps followed to define the elements of the optimization problems for noise and bandwidth stages. Furthermore, the two complete NLP problems are detailed. The two techniques used to solve each one of the problems and their corresponding results are presented in Section 4. Finally, some conclusions and future work are established in

Section 5.

2 Structured Electronic Design

In the 90's, a new design methodology was created, the Structured Electronic Design, which starts with an ideal solution based on the nullor. This means the amplifier does not produce noise, does not have distortion and its bandwidth is infinite. However, the nullor is an ideal device and must be replaced by a real one, which is a bipolar transistor (see Figure 2). This change is applied at each stage that composes the design process.

There are three assumptions, which are the basis for the methodology:

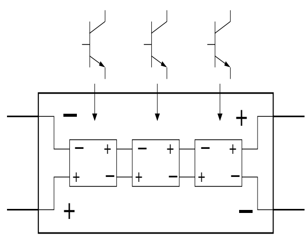

Figure 2. Each stage is represented by a nullor which is replaced by a transistor.

Orthogonality. The aspects to be optimized are assumed to have minima in one single direction, which allows as to design every stage independently.

Simplicity. The design procedure generates simple models, starting by ideal ones, because in this way the dependency of the functions to be optimized are limited to a small set of parameters.

Hierarchy. It reduces the complexity of the design problem by splitting it into independent problems that are solved in a given order.

Regarding amplifiers, the stages that compose the Structured Electronic Design are:

Noise. The noise is a non desired signal, which is found in the input of an amplifier. In this stage, the amount of noise that produces the amplifiers is estimated by equations 1 and 2 [7, 4].

* For the voltage amplifier

$$u_{n,u_{total}} = u_{ns} + u_{nn} + \left(R_s + \frac{R_1 R_2}{R_1+R_2}\right)^2 i_{nn} + \left(\frac{R_2}{R_1+R_2}\right)^2 u_{nR_1} + \left(\frac{R_1}{R_1+R_2}\right)^2 u_{nR_2} \quad (1)$$

* For the current amplifier

$$i_{n,i_{total}} = i_{ns} + i_{nn} + \left(\frac{1}{R_s} + \frac{1}{R_1+R_2}\right)^2 u_{nn} + \left(\frac{R_1}{R_1+R_2}\right)^2 i_{nR_1} + \left(\frac{R_2}{R_1+R_2}\right)^2 i_{nR_2} \quad (2)$$

where $u_{n,u_{total}}$ and $i_{n,i_{total}}$ are the whole noise of the amplifier; u_{ns} and i_{ns} are the voltage and current sources of the source resistor R_s; u_{nn} and i_{nn} are the noise sources of voltage and current associated to the *nullor*; R_1, R_2 are the resistive devices on the feedback network; R_s is the input resistive; i_{nR_1}, i_{nR_2}, u_{nR_1} and u_{nR_2} are the noise source associate to R_1 y R_2.

In this stage the nullor is replace by a transistor, which produces noise, the equations are associated to transistors depending on the configuration employed on the amplifier.

Common emitter

$$u_{nn} = 4kTr_b + \left(\frac{1}{g_m}\right)^2 2qI_c \qquad i_{nn} = 2qI_b + \left(\frac{1}{\beta}\right)^2 2qI_c \quad (3)$$

Common collector

$$u_{nn} = \left(\frac{r_\Pi}{1+\beta}\right)^2 2qI_c \left(\frac{\beta+1}{\beta}\right)^2 + 4kTr_b \qquad i_{nn} = \frac{4qI_c}{(\beta+1)^2} \quad (4)$$

Common base

$$u_{nn} = \left(\frac{g_m r_o}{1+g_m r_o}\right)^2 4kTr_b + \left(\frac{r_o}{1+g_m r_o}\right)^2 2qI_c \qquad i_{nn} = \left(\frac{1}{r_\pi+\beta r_o}\right)^2 4kTr_b + \left(\frac{r_o}{r_\pi+\beta r_o}\right)^2 2qI_c + 2qI_b \quad (5)$$

where k, T and q are the Boltzmann constant, the absolute temperature and the electron charge respectively. The parameters of the transistor are r_b and β. The small signal parameters of transistor are g_m, r_o and r_π. Besides, I_c and I_b represent the collector and base currents.

Distortion. The distortion affects the signal at the output, that concerns the changes or deformations that suffers the signal when it is amplified (see Figure 3). In this stage the current and voltage that satisfy user's requirement are calculated. All results in this stage are completely calculated in an analytic form (i.e. no parameter values search is required).

Bandwidth. Due to the fact that amplifiers use nullors, the bandwidth of amplifiers is infinite, changing when the

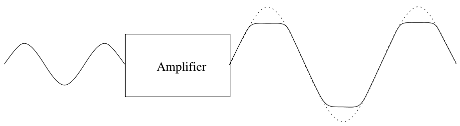

Figure 3. The input signal is cut in its valleys and crest with respect to input signal. It is a result of distortion.

nullors are replaced by transistors. In this stage, it is necessary to calculate the LP product in order to determine if the desired bandwidth can be achieved by the amplifier under design, i.e. if the maximax attainable frequency of the circuit is larger than the expected bandwidth. Furthermore, the poles of the final design must be placed on Butterworth's position [3].

3 Design optimization of negative feedback amplifiers

Recalling from last Section, the Structured Electronic Design promotes orthogonality (i.e. its stages are solved independently). Then, the NLP problems are formulated for two separated stages (noise and bandwidth) and their corresponding features. Distortion stage is not considered in this work because it is completely solved in an analytic form due to the fact that the values for the equations are known.

The optimization problem for noise stage is formulated in terms of equations 1 and 2. On the other hand, for the bandwidth stage, the objective is to reduce the distance between complex Butterworth position's and real position of the poles.

Deb, proposes a set of elements to be defined in order to get a NLP problem [2]: design variables, constraints, objective function and limits of variables. This methodology is followed in this work. The necessary elements to establish the NLP problems for noise and bandwidth stages are presented as follows.

3.1 Noise stage

For the noise stage, the objective is to find a transistor that produces a minimal noise and an appropriate range of I_c. Equations 1 and 2 are employed to calculate the noise and they depend on parameters that define the transistor and the value of elements of the feedback network (R_1 and R_2). The transistor replaces the nullor associated to this stage. Therefore, the design variables are: R_b, β, I_c and V_A. The graphic associated with these equations is given in Figure 4, where it can be observed that the noise spec is to an I_c's range.

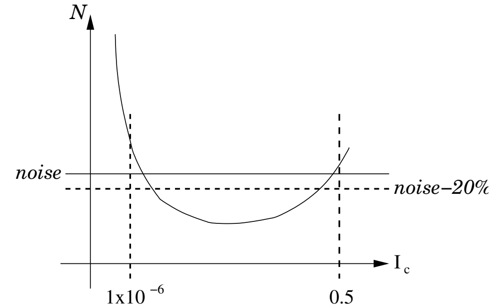

Figure 4. Representation of the curve associate to noise, where $noise$ is the requirement.

This problem has constraints, for example the minimum and maximum value for I_c; in this case they are 1×10^{-6} and 0.5. Furthermore, the noise value has to be lees than the 20% of the requirement, because the minimal point associated to the curve allows to choose other value (see Figure 4).

The optimization problem definition for noise stage is:

$$\text{Minimize } u_{n,u_{total}}|i_{n,i_{total}}$$

subject to:

$$\begin{array}{rcl} I_{c_1} & \geq & 1\times10^{-6} \\ I_{c_2} & \leq & 0.5 \\ u_{n,u_{total}}|i_{n,i_{total}} & < & noise - 20\% \end{array}$$

where I_{c_1} and I_{c_2} are the limits of I_c range, $u_{n,u_{total}}$ and $i_{n,i_{total}}$ are the noise produced by voltage and current amplifier, respectively.

The ranges of each variable are selected with regard to the values employed in transistor models commonly used, which are:

$$\begin{array}{ccccc} 1 & \leq & R_b & \leq & 300 \\ 100 & \leq & \beta & \leq & 400 \\ 1\times10^{-6} & \leq & I_c & \leq & 0.5 \\ 40 & \leq & V_A & \leq & 400 \end{array}$$

and the range associated to R_1 (element of the feedback network) is given considering the value of R_S:

Voltage amplifier

$$\frac{R_s}{10} \leq R_1 \leq 100R_s$$

Current amplifier

$$1 \leq R_1 \leq \frac{R_s}{20}$$

therefore, the variables used in the model are: R_b, β, I_c, V_A and R_1, taking real values.

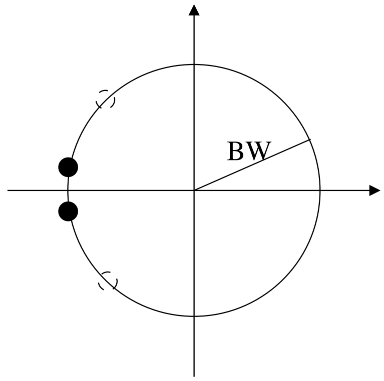

Figure 5. Two poles are on the circumference of radius bandwidth's requirement, their Butterworth's position are the dashed circles.

3.2 Bandwidth stage

For the bandwidth stage, the purpose is to put the poles in Butterworth's position by reducing the distance between the real angle and Butterworth's position. Figure 5 shows two poles on circumference of radius bandwidth's requirement although they aren't in Butterworth's position.

The poles are calculated with *libmna*[1]. The necessary parameters required to achieve compensation are: C_{ph} or L_{ph} (capacitors and inductors), depending on the amplifier type, in addition to I_{c_3} or I_c. The objective is to minimize the distance between the real position of poles and their Butterworth's position.

The optimization problem definition for bandwidth stage is:

$$\text{Minimize } diff\_ang$$

where $diff\_ang$ is the difference between real and correct angle.

The ranges of the variables are based on real values for these devices and the current is selected regarding the most appropriate behavior of the transistors. The ranges are:

Voltage amplifier

$$1 \times 10^{-15} \leq C_{ph} \leq 1 \times 10^{-12}$$

Current amplifier

$$1 \times 10^{-7} \leq L_{ph} \leq 1 \times 10^{-3}$$
$$1 \times 10^{-7} \leq I_{c_3} \leq 0.5$$

I_c has the range obtained in noise stage.

[1] A library of Maple developed by Roberto Castañeda, PhD student at INAOE.

4 Optimization results

4.1 Optimization techniques used

Two different approaches were used to solve each NLP problem. For the noise stage, Differential Evolution (DE) for constrained optimization [5] was chosen. DE is a novel evolutionary heuristic proposed by Price and Storn [6] which evolves a population of solutions by using a mutation operator based on the distribution of solutions in the search space. Four parameters must be defined by the user: the number of solutions in the population NP, the number of generations (iterations) to perform MAX_GEN, the scaling factor for the mutation operator F and the crossover probability CR. We selected DE for this stage because the performance of the mathematical programming method selected for this work (Hooke-Jeeves) [2], was too sensitive to: (1) the starting point and (2) the penalty values related with the constraint-handling. Furthermore, DE is one of the most recent evolutionary algorithms and has shown a very competitive performance when solving several optimization problems in different areas [6], it has shown a low sensitivity to its parameter values [5] and it is very easy to implement. To deal with the constraints of the problem, a set of simple criteria based on feasibility (originally proposed in [1]) were used [5].

The bandwidth stage was modeled as a unconstrained optimization problem, then, we used the Hooke-Jeeves pattern search method [2]. This approach provided a very competitive performance and it was not very sensitive to its initial search point. Three parameters must be tuned by the user: The variable increments Δ_i, $i = 1, 2, \ldots, n$ (where n is the number of decision variables), the step reduction factor α which aims to reduce the increments during the process and a small lower bound for the increments as a termination criterion ϵ. The use of an heuristic was not necessary in this case because Hooke-Jeeves was very competitive and easy to implement.

4.2 Experimental design

The parameter values used in each method were chosen empirically and are shown in Table 1.

Table 1. Parameter's values of methods use to solve optimization problems.

ED		Hooke-Jeeves	
F=0.75	CR=0.001	$\alpha = 1.2$	$\epsilon = 1e$-11
NP=30	MAX_GEN=300	$\Delta_p = 5e$-5	$\Delta_i = 7.5e$-4

Table 2 presents the design specifications for the voltage and current amplifiers. It is important to mention that transistors with common emitter configuration are used in the experiments

Table 2. Amplifier's requirements design with Structured Electronic Design.

	Voltage amplifier	Current amplifier
Noise	12	10
Gain	15	100
R_s	40 Ω	7.5 $k\Omega$
V_{in}	1 mV	1 μA
BW	500 kHz	500 kHz
f_T	300×10^6	250×10^6
$clipping$	0%	0%
R_L	2 $k\Omega$	3 $k\Omega$

The initial population for the DE algorithm was generated at random. However, with the aim to incorporate some knowledge about the problem to the search process, the values for R_b and β were generated inside the next intervals:

$$1 \leq R_b \leq 10$$
$$300 \leq \beta \leq 350$$

This modification in the intervals means that the combination of higher β values and lower R_b values generates little noise. The result of the optimization procedure yields a range for I_c that meets the noise spec as shown in Figure 4. The initial starting point for the Hooke-Jeeves method was also generated at random for the bandwidth stage. For each amplifier and for each stage, the optimization process was executed 30 times, either until a solution was found or the stop condition was fulfilled. We counted the number of evaluations performed because it is commonly used in the specialized literature as a measure (hardware-independent) to compare the computational cost of optimization methods [5].

4.3 Results

Table 3 shows the statistical results with respect to the number of evaluations of the objective function performed for the noise stage NLP problem. The first column corresponds to the voltage amplifier and the second column to the current amplifier. A run is successful if at least a feasible solution is found. The algorithm is able to always find a solution and the number of evaluations performed is smaller for the current amplifier than for the voltage amplifier.

Table 4 includes the best and worst results with respect to the noise and range of I_c obtained in the independent runs for the voltage amplifier. Also, Table 5 presents the results for the current amplifier.

Table 3. Statistical results for the number of evaluations performed by DE in the noise stage to the voltage and current amplifiers.

	Amplifier	
	Voltage	Current
Runs performed	30	30
Min. Evaluations	330	2
Max. Evaluations	1,020	22
Average Evaluations	20.6	12.97
Percentage of successful runs	100 %	100 %

Table 4. The best and worst values found by voltage amplifier in noise stage.

	$u_{n,u_{total}}$	Range of I_c
Best valor	6.34e-18	2.88e-1
Worse valor	7.83e-18	4.93e-1
Average	7.23e-18	4.07e-1
Median	7.30e-18	4.16e-1

The results obtained with DE for noise stage are good for both amplifiers and always found a feasible solution, including the best and worst solutions.

Table 6 summarizes the results with respect to the number of evaluations performed by the Hooke-Jeeves method for the bandwidth stage model for the voltage and the current amplifiers. A run is considered successful is the objective function value is less than 1, which means that the position reached is close to the optimum one.

As it can be noted, the number of evaluations computed for the voltage amplifier is higher than those required by the current amplifier. At the same time, the percentage of successful runs is better in the voltage that in current amplifier.

Table 7 contains the maximum and minimum distance between the real and Butterworth positions of poles, which are acceptable in both type of amplifiers. However, the difference is less in the current than in the voltage amplifier.

The values of the best solution in the bandwidth stage for each amplifier are shown in Table 8,where for the current amplifier, the device is L_{ph} and for the voltage amplifier

Table 5. The best and worst values found for the current amplifier in noise stage.

	$i_{n,i_{total}}$	Range of I_c
Best value	6.60e-24	2.11e-1
Worse value	1.58e-23	4.95e-1
Average	1.36e-23	3.94e-1
Median	1.51e-23	4.12e-1

Table 6. Statistical results for the number of evaluations performed by the Hooke-Jeeves method in the bandwidth stage for the voltage and current amplifiers.

	Amplifier	
	Voltage	Current
Runs performed	30	30
Min. evaluations	2,084	156
Max. evaluations	12,476	2,760
Average evaluations	6,078.21	1,120
Median	5,348	1, 000
Percentage of successful runs	93.33 %	76.67 %

Table 7. The maximum, minimum and average differences found in bandwidth stage on 30 runs.

	Amplifier	
	Voltage	Current
Maximum	6.50e-2	1.54e-4
Minimum	4.74e-2	1.81e-5
Average	5.64e-2	9.60e-5

is C_{ph}. These results are very competitive and adequate. Based on them, we can state that the proposed model as an NLP problem is working well.

Table 8. The best solutions for the voltage and the current amplifier in bandwidth stage.

	C_{ph}/L_{ph}	I_c	$diff\_ang$
Voltage amplifier	7.03e-15	2.76e-4	6.50e-2
Current amplifier	6.81e-7	1.14e-1	1.53e-4

5 Conclusions

In this work, two stages in Structured Electronic Design were modeled as numerical optimization problems. This process was possible because the devices associated to each stage can be related to the parameters involved in the problem definition. A valuable aspect of this current contribution is that the designer does not need to be an expert as to find an adequate transistor because the search process will do it for him. From the results obtained in the noise stage, it was noticed that the transistor must produce a small amount of noise and its I_c range has to be wide. In this noise stage the search was made with the Differential Evolution algorithm and its performance was very competitive, reaching feasible solutions in each single run. For the bandwidth stage, the problem was solved with the Hooke-Jeeves method because it is one of the most competitive direct methods (without using gradient information) for unconstrained optimization. The performance was also very competitive, but it required a higher number of evaluations with respect to the noise stage. The overall performance seems to indicate that the NLP problems introduced in this work provide a practical way to improve the design process of amplifiers without requiring expert knowledge from the designer. In fact, the obtained results are similar to those obtained by an expert designer, but in this case, the design values are now searched by the optimization techniques. Part of the future work includes the use of different configurations for the transistors and also the use of other optimization algorithms which may provide competitive results but with a lower number of evaluations of the objective function.

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